to: (a) prove the primary reference contains an enabled disclosure; (b) explain the meaning of a term used in the primary reference; or (c) show that a characteristic not disclosed in the reference is inherent.

It is unclear to Applicants for which (if any) of these three reasons the additional reference is cited. So that the record is clear, Applicants respectfully request clarification as to the reasoning why an extra reference is relied on in the rejection of claims 1-64 under 35 U.S.C. §102(b).

B. Neither Reference Discloses or Suggests Transmitting An Operand Address From A Process To A Debug Circuit

Each independent claim includes a limitation that relates to a processor configured to transmit to a debug circuit an operand address that indicates a memory location at which an operand value is stored. Neither MotorolaPAT nor MotorolaNPL discloses any such limitation.

1. *MotorolaPAT*

During the lengthy prosecution of this application, Applicants have repeatedly pointed out that MotorlaPAT (U.S. Patent No. 5,737,516) does not disclose or suggest transmitting an operand address from processor core 9 to debug circuit 10. Indeed, this was Applicants' primary argument in Applicants' appeal brief mailed September 18, 2006 (in response to which the Examiner elected to reopen prosecution, rather than file a reply brief).

Now, the Office Action appears to cite col. 20, lines 54-59, col. 14, lines 65-67, and col. 15, lines 1-23 of MotorolaPAT as purportedly disclosing that an operand address is transmitted from processor core 9 to debug circuit 10. Applicants continue to disagree that MotorolaPAT even remotely discloses or suggests that an operand address is transmitted from the processor core 9 to debug circuit 10.

As discussed in Applicants' appeal brief and numerous responses filed prior thereto, MotorolaPAT discloses that there are only five signals that can be transmitted from the processor core to the debug circuit. These signals are Bus Grant, CPST, KADDR, KDATA, and KCONTROL. MotorolaPAT does not disclose or suggest that any of the signals sent from processor core 9 to debug module 10 include an operand address.

Although the KADDR signal may include instruction addresses, instruction addresses are very different from operand addresses. That is, an instruction address specifies the memory location of an instruction stored in memory, whereas an operand address specifies the memory

location of an operand value stored in memory. In addition, although the KDATA signal of the system of MotorolaPAT permits operand values to be transmitted from the processor core to the debug module. However, an operand value is very different from an operand address. That is, an operand address is the memory location in which an operand value is stored.

Moreover, none of the above-mentioned portions of MotorolaPAT cited in the Office Action are even remotely related to transmitting an operand address from a processor to a debug circuit. Specifically, col. 20, lines 54-59 relate to the PST and DDATA signals. However, these signals are not transmitted from a processor to a debug circuit, but rather are transmitted from the debug circuit to an external development system. Specifically, Figure 1 of MotorolaPAT shows that debug module 10 transmits the DDATA and PST signals to external development system 7.

At col. 14, lines 65-67, MotorolaPAT states, "[t]he present invention provides an important and hereto non-existent, real time trace function." This sentence does not disclose or suggest that an operand address is transmitted from a processor to debug circuit.

Col. 15, lines 1-23 discuss the DDATA and PST signals. As should be clear from the discussion above, these signals are not transmitted from a processor to a debug circuit, but rather are transmitted from the debug circuit to an external development system.

As should be clear from the discussion above, MotorolaPAT does not disclose or suggest that an operand address is transmitted from the processor to the debug circuit.

2. *MotorolaNPL*

MotorolaNPL also fails to disclose or suggest that an operand address is transmitted from a processor to a debug circuit. The Office Action cites section 3 on page 4 and Figure 7 on page of the reference as purportedly disclosing this. Applicants respectfully disagree.

The section of the MotorolaNPL cited in the Office Action relates to the information transmitted by the DDATA and PST signals. The Office Action alleges that an operand address may be transmitted on the DDATA signal. Applicants respectfully disagree. However, even if it is assumed that an operand address is transmitted via the DDATA signal (though clearly it is not), MotorolaNPL still fails to disclose or suggest that an operand address is transmitted from a processor to a debug circuit, **as the DDATA signal is not transmitted from a processor to a debug circuit**.

Rather, as shown in Figure 3 (page 2) and Figure 4 (page 3), the DDATA signal is output by the debug module and is not transmitted from the processor core to the debug module. Indeed, in section 3 on page 4, MotorolaNPL makes clear that the DDATA and PST signals are

transmitted from the debug module to an external development system, stating, "[w]hen connected to an external development system, the PST/DDATA port provides a useful debug utility in tracking the dynamic execution path of instructions."

As should be clear from the discussion above, MotorolaNPL does not disclose or suggest that an operand address is transmitted from the processor to the debug circuit. As neither MotorolaPAT nor MotorlaNPL discloses or suggests that an operand address is transmitted from the processor to the debug circuit, it is respectfully requested that the rejection of claims 1-64 under 35 U.S.C. §102(b) be withdrawn.

CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Dated: October 15, 2007

Respectfully submitted,

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